EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Clingan Jim, Reg. No. 30,163 on 02/25/2008.

The application has been amended claim 16 as follows:

16. (currently amended) A high speed circuit for performing an arithmetic function comprising one of a group consisting of division and square root applied to a number and provide a result of the arithmetic function based on partial iterations, comprising:

a counter for providing a count to identify a current partial iteration;

a comparator having a first input for receiving the number, a second input, and an output;

register means~~, having a first input coupled to the output of the comparator, a second input coupled to the counter, and an output, wherein the register means is~~ for storing a current estimate of the result of the arithmetic function as applied to the number based on previous partial iterations, for providing an output representative of a next partial iteration, and for updating the result based on the output of the

comparator, wherein the register means has a first input coupled to the output of the comparator, a second input coupled to the counter, and an output;

storage means for storing an inverse of the arithmetic function of the current estimate and having an output on which is provided the inverse of the arithmetic function of the current estimate of the result;

incremental means having an input coupled to the output of the register means for providing, on an output, an incremental effect, wherein the incremental effect is a value that when added to the inverse of the mathematical function of the current estimate is equal to the inverse function of a next current estimate plus the next partial iteration; and

summing means, having an output coupled to the second input of the comparator, a first input coupled to the output of the storage means, a second input coupled to the incremental means, for providing on the output a sum of the incremental effect and the inverse of the arithmetic function of the current estimate.

2. Claims 16-18 are allowed.

3. Claims 1-15 and 19-23 are cancelled.

4. The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose or render an obviousness of a detail structure of a high-speed circuit for performing an arithmetic function comprising: a

counter for providing a count to identify a current partial iteration; a comparator having a first input for receiving the number, a second input, and an output; register means has a first input coupled to the output of the comparator, a second input coupled to the counter, and an output; storage means for storing an inverse of the arithmetic function of the current estimate and having an output on which is provided the inverse of the arithmetic function of the current estimate of the result; incremental means having an input coupled to the output of the register means; and summing means, having an output coupled to the second input of the comparator, a first input coupled to the output of the storage means, a second input coupled to the incremental means as cited in an independent claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

February 29, 2008

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/730,174	ZOSO ET AL.	
	Examiner	Art Unit	
	CHAT C. DO	2193	